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Title: **IMPROVED APPARATUS AND METHOD FOR PERFORMING IMPEDANCE MEASUREMENTS**

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Title: IMPROVED APPARATUS AND METHOD FOR PERFORMING IMPEDANCE MEASUREMENTS

Cross Reference To Related Application

[0001] This application claims priority from provisional application serial no. 60/429,316 filed November 27, 2002.

Field of the invention

[0002] This invention relates to a system for medical diagnosis of disease and specifically relates to a system for measuring electrical impedances of body parts to diagnose medical disease.

Background of the invention

[0003] The onset of disease is often accompanied by physical changes in a body part. Some physical changes, while not discernible by a patient, can be detected with appropriate diagnostic equipment, often at a relatively early stage of the disease.

[0004] For example, the electrical impedances of various body tissues are well known through studies on intact humans or from excised tissue made available following therapeutic surgical procedures. In addition, it is well documented that a decrease in electrical impedance occurs in tissue as it undergoes cancerous changes. This finding is consistent over many animal species and tissue types, including, for example human breast cancers. Consequently, electrical impedance may be used to diagnose disease.

[0005] A method that permits comparisons of electrical properties for diagnostic purposes has been developed that involves homologous body parts, i.e., body parts that are substantially similar, such as a left breast and a right breast. In this method, the impedance of a body part of a patient is compared to the impedance of the homologous body part of the *same* patient. One technique for screening and diagnosing diseased states within the body using electrical impedance is disclosed in U.S. Pat. No. 6,122,544, which is incorporated herein by reference. In this patent, data are obtained from two anatomically homologous body regions, one of which may be affected by

disease. Differences in the electrical properties of the two homologous body parts could signal disease.

[0006] Published international patent application, PCT/CA01/01788, which is incorporated herein by reference, discloses a breast electrode array for diagnosing the presence of a disease state in a living organism, wherein the electrode array comprises a flexible body, a plurality of flexible arms extending from the body, and a plurality of electrodes provided by the plurality of flexible arms, wherein the electrodes are arranged on the arms to obtain impedance measurements between respective electrodes. In one embodiment, the plurality of flexible arms are spaced around the flexible body and are provided with electrode pairs, which can be used to make tetrapolar impedance measurements.

[0007] Tetrapolar impedance measurements are associated with injecting current between so called current injection electrodes and measuring a voltage drop between associated electrodes. In a preferred embodiment, the differences between corresponding homologous impedance measurements in the two body parts are compared in a variety of ways that allows the calculation of metrics that can serve either as an indicator of the presence of disease or to localize the disease to a specific breast quadrant or sector.

__Summary of the invention__

[0008] In an RC circuit, the impedance *Z*, is a complex number, whose real part is the resistance *R* and whose imaginary part is the capacitive reactance $X_C = (\omega C)^{-1}$, where ω is the frequency at which the voltage (or current) oscillates and *C* is the capacitance of the circuit. The magnitude of the impedance *Z* is given by: $|Z| = |V| / |I|$, and the phase, ϕ, of the impedance *Z* is given by: $|\phi| = |\arg(V) - \arg(I)| = \left|\tan^{-1}[X_C(\omega)/R]\right|$, where *I* denotes the current and *V* denotes the voltage.

[0009] A bioelectrical impedance diagnostic system can be used to measure several impedances of a body part, such as a human breast, to

diagnose the possibility of disease therein. The diagnostic system includes various leads that connect to the body part via electrodes. The leads are used to inject current and to measure resultant voltages; the currents and voltages thereafter being used to calculate impedances. These impedances may then be used for diagnostic purposes because as disease in a body part progresses, the impedance of the body part changes in a predictable fashion. The greater the number of impedances obtained for different electrical pathways, the better the diagnosis can be.

[0010] In a first aspect, the present invention provides a system for detecting the possibility of disease in one of a first body part and a second substantially similar body part by impedance measurements. The system comprises a main module for controlling the operation of the system, and a front-end module connected to the main module and at least one of the first and second body parts for injecting stimulus currents into the at least one of the first and second body parts and receiving voltages generated by the at least one of the first and second body parts in response to the stimulus currents. The system further comprises an impedance module connected to the main module and the front-end module for creating the stimulus currents and determining the impedance of the at least one of the first and second body parts based on the received voltages. The stimulus currents comprise a current signal and a complementary current signal thereby forming a differential current signal.

[0011] The impedance module preferably comprises a current generator for generating the stimulus currents. The current generator includes a first current generation module for generating an internal current signal; a first output impedance unit connected to the first current generation module for generating the current signal based on the internal current signal; a second current generation module connected to the first current generation module for generating an internal complementary current signal; and, a second output impedance unit connected to the second current generation

module for generating the complementary current signal based on the internal complementary current signal.

[0012] The current generator further may comprise a first current shield generator for generating a current shield signal related to the current signal; and, a second current shield generator for generating a complementary current shield signal related to the complementary current signal. The current shield signal and complementary current shield signals are provided to the front-end module to shield the current signal and complementary current signal from noise. The first current shield generator preferably includes an amplifier having a gain factor for amplifying the current signal to generate the current shield signal, the gain factor being chosen to provide a negative capacitance. The second current shield generator preferably includes an amplifier having a gain factor for amplifying the complementary current signal to generate the complementary current shield signal, the gain factor being chosen to provide a negative capacitance.

[0013] The impedance module preferably further comprises a processing unit for creating a current control voltage signal for controlling parameters related to the stimulus currents; and, a digital-to-analog converter connected to the processing unit for receiving the current control voltage signal and generating an analog current control voltage signal. The current generator further preferably comprises a single-ended differential conversion unit connected to the digital-to-analog converter and the first current generation module for converting the analog current control voltage signal to a differential current control voltage signal.

[0014] Preferably, one of the parameters is frequency and the frequency of the generated stimulus currents is given by $F_n=F_1*K^n$ where K is a constant and n is an integer greater than or equal to 2.

[0015] The first current generation module comprises a first gain stage that includes an amplification stage for amplifying the differential current control voltage signal and converting the amplified differential current control voltage signal to a single-ended amplified current control voltage signal; a

filter stage connected to the amplification stage for filtering noise in the single-ended amplified current control voltage signal; and, a feedback stage connected to the amplification stage and the filter stage for feeding back an integrated version of the filtered single-ended amplified current control voltage signal to ensure that the single-ended amplified current control voltage is centered about ground.

[0016] The first current generation module further preferably comprises a current generation stage connected to the first gain stage for creating the internal current signal. The current generation stage includes a second amplification stage for amplifying a difference between the filtered single-ended amplified current control voltage and an integrated version of the internal current signal to generate the internal current signal; and, a second feedback stage connected to the second amplification stage for providing the integrated version of the internal current signal thereto. The second feedback stage includes a voltage follower connected to the second amplification stage for following the output of the second amplification stage; and, an integrator connected to the voltage follower and the second amplification stage for integrating the output of the voltage follower and providing the integrated output to the second amplification stage, the integrated output being the integrated version of the internal current signal.

[0017] The second current generation module comprises a phase adjusting stage for receiving the internal current signal and generating a phase-adjusted internal current signal; and, an inverting stage connected to the phase adjusting stage for inverting the phase-adjusted internal current signal to create the internal complementary current signal.

[0018] The impedance module further comprises a signal conditioning unit for pre-processing the received voltages to produce a single-ended processed measured voltage, the received voltages forming a differential signal and including a first measured voltage signal and a second measured voltage signal; and, a programmable gain unit connected to the signal conditioning unit for providing a plurality of gain levels to the single-ended

processed measured voltage to generate a single-ended amplified measured voltage, the gain levels being defined according to $G_n=G_1*K^n$ where K is a constant and n is an integer greater than or equal to 2.

[0019] The signal conditioning unit further comprises a first voltage shield generator for generating a first voltage shield signal related to the first measured voltage signal; and, a second voltage shield generator for generating a second voltage shield signal related to the second measured voltage signal. The first and second voltage shield signals are provided to the front-end module to shield the first and second measured voltage signals from noise. The first voltage shield generator preferably includes an amplifier having a gain factor for amplifying the first measured voltage signal to generate the first voltage shield signal, the gain factor being chosen to provide a negative capacitance. The second voltage shield generator preferably includes an amplifier having a gain factor for amplifying the second measured voltage signal to generate the second voltage shield signal, the gain factor being chosen to provide a negative capacitance.

[0020] The signal conditioning unit comprises a differential input network including a first filtering stage for removing noise from the first and second measured voltage signals to generate first filtered measured voltages; a common-mode rejection stage connected to the first filtering stage for removing high frequency common mode noise to generate second filtered measured voltages; and, a second filter stage connected to the common-mode rejection stage for removing noise from the second filtered measured voltages. The signal conditioning unit further comprises a differential voltage amplifier including: an amplification stage for amplifying a difference between the second filtered measured voltages and generating a single-ended measured voltage signal; a filter stage connected to the amplification stage for filtering the single-ended measured voltage signal; and, a feedback stage connected to the amplification stage for providing an integrated version of the single-ended amplified measured voltage to the amplification stage.

[0021] The impedance module further comprises a processing unit for calculating impedance values based on the stimulus currents and a corresponding digitized single-ended measured voltage signal; and an analog-to-digital converter connected to the processing unit for converting the single-ended measured voltage signal to create the digitized single-ended measured voltage signal. The programmable gain unit comprises a programmable gain amplifier including: an amplification stage for amplifying the filtered single-ended measured voltage signal; a second filter stage connected to the amplification stage for filtering the output of the amplification stage; and, a variable resistance stage connected to the amplification stage for providing the plurality of gain levels, the variable resistance stage including a multiplexer and a plurality of resistor configurations connected to the output paths of the multiplexer; each resistor configuration being related to each other by the factor K. The programmable gain amplifier further comprises an output stage connected to the programmable gain amplifier for amplifying and shifting the DC level of the output of the second filter stage to create the single-ended amplified measured voltage.

[0022] The signal conditioning unit preferably includes a common-mode voltage measurement stage for measuring a common-mode voltage of the received voltages. The impedance module further includes a processing unit comprising: a calculator module for calculating impedance values based on the stimulus currents and the received voltages; and, a calibrator module for correcting the calculated impedance values, the calibrator module applying a common-mode calibration step and an impedance calibration step.

[0023] For a given calculated impedance value, the common-mode calibration step includes identifying the magnitude and phase of the measured common-mode voltage at a pre-defined measurement frequency and correcting the calculated impedance value by subtracting a weighted version of the measured common-mode voltage from the calculated impedance value, the weight being defined by the amount of common-mode voltage rejection provided by the signal conditioning unit.

[0024] Alternatively, for a given calculated impedance value, the common-mode calibration step includes identifying the magnitude and phase of the measured common-mode voltage at a pre-defined measurement frequency and correcting the calculated impedance value by subtracting a common-mode calibration number obtained from a lookup table, the common-mode calibration value being indexed by the magnitude and phase of the measured common-mode voltage.

[0025] For a given calculated impedance value, the impedance calibration step includes correcting the calculated impedance value by applying an impedance calibration factor from a calibration table, the impedance calibration factor being indexed by the gain that is applied by the programmable gain unit, the measurement frequency and the magnitude of the calculated impedance value. The impedance calibration factor may also be indexed by the phase of the calculated impedance value.

[0026] The system further includes a calibration board for generating the calibration table, the calibration board including a plurality of calibration resistors and a plurality of calibration capacitors selectively connectable with one another to form a plurality of calibration impedances, wherein the resistance of the plurality of calibration resistors are related to one another according to $R_n=R_1*K^n$ and the capacitance of the calibration capacitors are related to one another according to $C_n=C_1*K^n$ and calibration is performed at calibration frequencies related to one another according to $F_n=F_1*K^n$.

[0027] The system as defined above can be used for detecting the possibility of disease in a patient.

[0028] In a second aspect, the present invention provides an impedance module for calculating the impedance of a body part, the impedance module creating stimulus currents for injection into the body part and receiving voltages generated by the body part in response to the stimulus currents. The impedance module comprises a current generator for generating the stimulus currents, the stimulus currents comprising a current signal and a complementary current signal thereby forming a differential

current signal; voltage processing circuitry for pre-processing the received voltages and amplifying the received voltages to generate a measured voltage signal; and, processing circuitry connected to the current generator and the voltage processing circuitry for directing the operation of the impedance module, the processing circuitry including a processing unit for creating a current control voltage signal for controlling parameters related to the stimulus currents, and for calculating an impedance value based on the stimulus current and the measured voltage signal; and, interface circuitry connected to the current generator, the voltage processing circuitry and the processing circuitry.

[0029] The current generator comprises: a first current generation module for generating an internal current signal; a first output impedance unit connected to the first current generation module for generating the current signal based on the internal current signal; a second current generation module connected to the first current generation module for generating an internal complementary current signal; and, a second output impedance unit connected to the second current generation module for generating the complementary current signal based on the internal complementary current signal.

[0030] The current generator further comprises: a first current shield generator for generating a current shield signal related to the current signal; and, a second current shield generator for generating a complementary current shield signal related to the complementary current signal. In use, the current shield signal and complementary current shield signals are used to shield the current signal and complementary current signal from noise. The first current shield generator includes an amplifier having a gain factor for amplifying the current signal to generate the current shield signal, the gain factor being chosen to provide a negative capacitance. The second current shield generator includes an amplifier having a gain factor for amplifying the complementary current signal to generate the complementary current shield signal, the gain factor being chosen to provide a negative capacitance.

[0031] The interface circuitry comprises a digital-to-analog converter connected to the processing unit for receiving the current control voltage signal and generating an analog current control voltage signal. The current generator further comprises a single-ended differential conversion unit connected to the digital-to-analog converter and the first current generation module for converting the analog current control voltage signal to a differential current control voltage signal.

[0032] One of the parameters is frequency and the frequency of the generated stimulus currents is given by $F_n=F_1*K^n$ where K is a constant and n is an integer greater than or equal to 2.

[0033] The first current generation module comprises a first gain stage comprising an amplification stage for amplifying the differential current control voltage signal and converting the amplified differential current control voltage signal to a single-ended amplified current control voltage signal; a filter stage connected to the amplification stage for filtering noise in the single-ended amplified current control voltage signal; and, a feedback stage connected to the amplification stage and the filter stage for feeding back an integrated version of the filtered single-ended amplified current control voltage signal to ensure that the single-ended amplified current control voltage is centered about ground.

[0034] The first current generation module further comprises a current generation stage connected to the first gain stage for creating the internal current signal, the current generation stage comprising: a second amplification stage for amplifying a difference between the filtered single-ended amplified current control voltage and an integrated version of the internal current signal to generate the internal current signal; and, a second feedback stage connected to the second amplification stage for providing the integrated version of the internal current signal thereto. The second feedback stage comprising: a voltage follower connected to the second amplification stage for following the output of the second amplification stage; and, an integrator connected to the voltage follower and the second amplification

stage for integrating the output of the voltage follower and providing the integrated output to the second amplification stage, the integrated output being the integrated version of the internal current signal.

[0035] The second current generation module comprises: a phase adjusting stage for receiving the internal current signal and generating a phase-adjusted internal current signal; and, an inverting stage connected to the phase adjusting stage for inverting the phase-adjusted internal current signal to create the internal complementary current signal.

[0036] The voltage processing circuitry comprises: a signal conditioning unit for pre-processing the received voltages to produce a single-ended processed measured voltage, the received voltages forming a differential signal and including a first measured voltage signal and a second measured voltage signal; and, a programmable gain unit connected to the signal conditioning unit for providing a plurality of gain levels to the single-ended processed measured voltage to generate a single-ended amplified measured voltage, the gain levels being defined according to $G_n=G_1*K^n$ where K is a constant and n is an integer greater than or equal to 2.

[0037] The signal conditioning unit optionally comprises: a first voltage shield generator for generating a first voltage shield signal related to the first measured voltage signal; and, a second voltage shield generator for generating a second voltage shield signal related to the second measured voltage signal. In use, the first and second voltage shield signals shield the first and second measured voltage signals from noise. The first voltage shield generator includes an amplifier having a gain factor for amplifying the first measured voltage signal to generate the first voltage shield signal, the gain factor being chosen to provide a negative capacitance. The second voltage shield generator includes an amplifier having a gain factor for amplifying the second measured voltage signal to generate the second voltage shield signal, the gain factor being chosen to provide a negative capacitance.

[0038] The signal conditioning unit comprises a differential input network including: a first filtering stage for removing noise from the first and

second measured voltage signals to generate first filtered measured voltages; a common-mode rejection stage connected to the first filtering stage for removing high frequency common mode noise to generate second filtered measured voltages; and, a second filter stage connected to the common-mode rejection stage for removing noise from the second filtered measured voltages. The signal conditioning unit also includes a differential voltage amplifier including: an amplification stage for amplifying a difference between the second filtered measured voltages and generating a single-ended measured voltage signal; a filter stage connected to the amplification stage for filtering the single-ended measured voltage signal; and, a feedback stage connected to the amplification stage for providing an integrated version of the single-ended amplified measured voltage to the amplification stage.

[0039] The interface circuitry further comprises an analog-to-digital converter connected to the processing unit for converting the single-ended measured voltage signal to create the digitized single-ended measured voltage signal. The programmable gain unit comprises a programmable gain amplifier including: an amplification stage for amplifying the filtered single-ended measured voltage signal; a second filter stage connected to the amplification stage for filtering the output of the amplification stage; and, a variable resistance stage connected to the amplification stage for providing the plurality of gain levels, the variable resistance stage including a multiplexer and a plurality of resistor configurations connected to the output paths of the multiplexer; each resistor configuration being related to each other by the factor K. The programmable gain unit also comprises an output stage connected to the programmable gain amplifier for amplifying and shifting the DC level of the output of the second filter stage to create the single-ended amplified measured voltage.

[0040] The signal conditioning unit includes a common-mode voltage measurement stage for measuring a common-mode voltage of the received voltages, and the processing unit includes: a calculator module for calculating the impedance value; and, a calibrator module for correcting the calculated

impedance value, the calibrator module applying a common-mode calibration step and an impedance calibration step.

[0041] For a given calculated impedance value, the common-mode calibration step includes identifying the magnitude and phase of the measured common-mode voltage at a pre-defined measurement frequency and correcting the calculated impedance value by subtracting a weighted version of the measured common-mode voltage from the calculated impedance value, the weight being defined by the amount of common-mode voltage rejection provided by the signal conditioning unit.

[0042] Alternatively, for a given calculated impedance value, the common-mode calibration step includes identifying the magnitude and phase of the measured common-mode voltage at a pre-defined measurement frequency and correcting the calculated impedance value by subtracting a common-mode calibration value from a lookup table, the common-mode calibration value being indexed by the magnitude and phase of the measured common-mode voltage.

[0043] For a given calculated impedance value, the impedance calibration step includes correcting the calculated impedance value by applying an impedance calibration factor from a calibration table, the impedance calibration factor being indexed by the gain that is applied by the programmable gain unit, the measurement frequency and the magnitude of the calculated impedance value. The impedance calibration factor may also be indexed by the phase of the calculated impedance value.

[0044] The impedance module is connectable to a calibration board for generating the calibration table, the calibration board including a plurality of calibration resistors and a plurality of calibration capacitors selectively connectable with one another to form a plurality of calibration impedances, wherein the resistance of the plurality of calibration resistors are related to one another according to $R_n=R_1*K^n$ and the capacitance of the calibration capacitors are related to one another according to $C_n=C_1*K^n$ and calibration is

performed at calibration frequencies related to one another according to $F_n=F_1*K^n$.

[0045] The impedance module as defined above can be used for calculating the impedance of a body part of a patient or other biological entity.

[0046] In a third aspect, the present invention provides a method of calculating the impedance of a body part, the method comprising:

a) providing stimulus currents for injection into the body part, the stimulus currents comprising a current signal and a complementary current signal thereby forming a differential current signal;

b) receiving voltages generated by the body part in response to the stimulus currents;

c) pre-processing the received voltages and amplifying the received voltages to generate a measured voltage signal; and,

d) calculating an impedance value based on the stimulus currents and the measured voltage signal.

[0047] The complementary current signal is 180 degrees out of phase with respect to the current signal.

[0048] The step of providing the stimulus currents optionally includes generating a first current shield signal related to the current signal for shielding the first current signal, and a second current shield signal related to the complementary current signal for shielding the complementary current signal. The first current shield signal is related to the first current signal by a gain factor, the gain factor being chosen to provide a negative capacitance. The second current shield signal is related to the complementary current signal by a gain factor, the gain factor being chosen to provide a negative capacitance.

[0049] The frequency of the generated stimulus currents is given by $F_n=F_1*K^n$ where K is a constant and n is an integer greater than or equal to 2

and a plurality of gain levels are used for amplifying the received voltages, the gain levels being defined by $G_n=G_1*K^n$.

[0050] The received voltages form a differential pair including a first received voltage signal and a second received voltage signal, and the method further comprises optionally generating a first voltage shield signal related to the first received voltage signal for shielding the first received voltage signal, and generating a second voltage shield signal related for the second received voltage signal for shielding the second received voltage signal. The first voltage shield signal is related to the first received voltage signal by a gain factor, the gain factor being chosen to provide a negative capacitance. The second voltage shield signal is related to the second received voltage signal by a gain factor, the gain factor being chosen to provide a negative capacitance.

[0051] The step of pre-processing the received voltages includes measuring a common-mode voltage of the received voltages and calculating the impedance value includes correcting the calculated impedance value by applying a common-mode calibration step and an impedance calibration step.

[0052] For a given calculated impedance value, the common-mode calibration step includes identifying the magnitude and phase of the measured common-mode voltage at a pre-defined measurement frequency and correcting the calculated impedance value by subtracting a weighted version of the measured common-mode voltage from the calculated impedance value, the weight being defined by the amount of common-mode voltage rejection provided by the pre-processing step.

[0053] Alternatively, for a given calculated impedance value, the common-mode calibration step includes identifying the magnitude and phase of the measured common-mode voltage at a pre-defined measurement frequency and correcting the calculated impedance value by subtracting a common-mode calibration value obtained from a lookup table, the common-mode calibration value being indexed by the magnitude and phase of the measured common-mode voltage.

[0054] For a given calculated impedance value, the impedance calibration step includes correcting the calculated impedance value by applying an impedance calibration factor from a calibration table, the impedance calibration value factor being indexed by the gain level, the measurement frequency and the magnitude of the calculated impedance value. The impedance calibration factor may also be indexed by the phase of the calculated impedance value.

[0055] The method as defined above can be used for calculating the impedance of a body part of a patient or other biological entity.

Brief description of the drawings

[0056] For a better understanding of the present invention and to show more clearly how it may be carried into effect, reference will now be made, by way of example only, to the accompanying drawings which show an exemplary embodiment of the present invention and in which:

[0057] Figure 1 is a block diagram of a medical diagnostic system for diagnosing the possibility of disease;

[0058] Figure 2 is a block diagram of an impedance module of the medical diagnostic system of Figure 1;

[0059] Figure 3a is a block diagram of a current generator of the impedance module of Figure 2;

[0060] Figure 3b is a circuit schematic of the single-ended to differential conversion unit of the current generator of Figure 3a;

[0061] Figure 3c is a circuit schematic of the first current generation module of the current generator of Figure 3a;

[0062] Figure 3d is a circuit schematic of the second current generation module of the current generator of Figure 3a;

[0063] Figure 3e is a circuit schematic of the output impedance network of the current generator of Figure 3a;

[0064] Figure 3f is a circuit schematic of the current shield generator of the current generator of Figure 3a;

[0065] Figures 3g-1 and 3g-2 show a circuit schematic of the exemplary embodiments of the sub-blocks of the current generator of Figure 3a;

[0066] Figure 4a is a block diagram of the voltage processing modules of the impedance module of Figure 2;

[0067] Figure 4b is a circuit schematic of the differential input network of Figure 4a;

[0068] Figure 5c is a circuit schematic of the differential voltage amplifier of Figure 4a;

[0069] Figure 5d is a circuit schematic of the programmable gain amplifier of Figure 4a;

[0070] Figure 4e is a circuit schematic of the output stage of Figure 4a; and,

[0071] Figures 4f-1 and 4f-2 show a circuit schematic showing of the exemplary embodiments of the components of the voltage processing modules of the impedance module of Figure 2.

Detailed description of the invention

[0072] Referring to Figure 1, shown therein is a medical diagnostic system **10** for diagnosing the possibility of disease in one of a first body part and a second substantially similar body part by utilizing impedance measurements. The first body part and the second substantially similar body part can be a homologous anatomical pair, such as, for example, a right breast (i.e. the first body part) and a left breast (i.e. the second body part). The medical diagnostic system **10** interfaces to the parallel and serial data ports of a computing device **12** by means of a parallel and serial data cable, respectively, shown collectively as connection cable **14** (standard IEEE-1284 parallel cables and RS-232 serial cables can be used). Alternatively, the

medical diagnostic system **10** may be modified to utilize a different means of connection to the computing device **12**, as is commonly known to those skilled in the art, such as a USB connection or the like. The computing device **12** may be a personal computer, laptop or other suitable computing device that is capable of running a medical diagnostic program **16** that employs the homologous impedance measurement method of detecting disease. The computing device **12** can also include means for printing and saving the data that is acquired by the medical diagnostic system **10**.

[0073] The medical diagnostic system **10** includes a main module **18**, an impedance module **20** and a front-end module **22**. The front-end module **22** interfaces to a first electrode array **24** and a second electrode array **26** via a first cable connector **28** and a second cable connector **30** respectively. The first and second cable connectors **28** and **30** may be ribbon cables or the like. The connectors **28** and **30** may be physically connected to one another at the ends that connect with the front-end module **22** and then split apart from one another at the ends that connect with the first and second electrode arrays **24** and **26**.

[0074] There are three types of signals pass through each electrode array **24** and **26**: current, voltage and ground signals. Conductors for the ground signals are placed, wherever possible, between conductors for every current and every voltage signal in order to isolate the current and voltage signals from each other. The ground signals also allow for an electrical test to confirm that the first and second electrode arrays **24** and **26** have been attached correctly to the cable connectors **28** and **30**.

[0075] The computing device **12**, when running the medical diagnostic program **16**, provides information signals to the medical diagnostic system **10**. In particular, the computing device **12** preferably provides information for measurements performed by the front-end module **22**, and the power delivered to the medical diagnostic system **10** via the parallel port. The parallel port is used to transfer data signals, control signals and status signals.

The computing device **12** also communicates with the impedance module **20** by signals transferred via the serial port.

[0076] The main module **18** controls the operation of the medical diagnostic system **10** and is responsible for system interface, power supply management, and electrical isolation. Accordingly, every other module (i.e. sub-system) of the medical diagnostic system **10** derives its power from the main module **18**. The impedance module **20** is responsible for generating currents and measuring voltage signals. The front-end module **22** is responsible for selecting the appropriate electrodes on the first and second electrode arrays **24** and **26** to which generated currents are sent to and measured voltage signals are obtained from. The first and second electrode arrays **24** and **26** are in contact with the respective body parts in order to obtain voltage measurements for calculating the impedances of those body parts.

[0077] The main module **18** includes an interface/control unit **32**, a power supply unit **34** and an isolation unit **36**. The interface/control unit **32** provides an interface between the computing device **12** and the medical diagnostic system **10**. In one embodiment, the interface/control unit **32** includes an RS-232 transceiver **38**, a parallel port power generator **40** and a diagnostic multiplexer **42**. The RS-232 transceiver **38** provides a bi-directional serial data link between the computing device **12** and the medical diagnostic system **10**.

[0078] The parallel port power generator **40** provides a parallel combination of several of the parallel-port signals to provide sufficient current to initiate the operation of an AC line switch **44** which resides within the power supply unit **34**. Accordingly, the computing device **12** controls the amount of power that is delivered to the rest of the medical diagnostic system **10** via the parallel port connection. When power is established in the medical device system **10**, a feedback connection can be used to maintain the power level. One bit may be used for this feedback.

[0079] The diagnostic multiplexer **42** provides status information regarding the status of the medical diagnostic system **10** to the medical diagnostic program **16**. The diagnostic multiplexer **42** can select diagnostic signals related to the connection between the computing device **14** and the main module **18** as well as the quality of the power supply voltages that are provided by the power supply unit **34**.

[0080] The power supply unit **34** provides power-supply verification and regulation for the other components of the medical diagnostic system **10**. In one embodiment, the power supply unit **34** comprises the AC line switch **44** which is connected to an AC/DC converter **46** by which AC power to the remainder of the medical diagnostic system **10** can be fully controlled. The AC line switch **44** is connected to the AC/DC converter **46** by a fuse **48** in order to provide an acceptable upper limit on the AC current that is provided to the AC/DC converter **46**. The AC/DC converter **46** preferably provides two channels of DC signals to the remainder of the medical diagnostic system **10**.

[0081] The isolation unit **36** electrically isolates the remainder of the medical diagnostic system **10** from the computing device **12** and the mains supply. Accordingly, the computing device **12** and a portion of the medical diagnostic system **10**, which includes the interface/control unit **32** and the power supply unit **34**, can be considered to be a ground side and the remainder of the medical diagnostic system **12** can be considered to be an isolated side. The isolation unit **36** comprises opto-couplers **48** through which data and control signals are exchanged between the isolated side and the ground-side. In one embodiment, the number of such signals is eight. The isolation unit **36** also includes an isolated DC/DC converter **50** to transfer power from the ground-side to the isolated side. Accordingly, the power that is supplied to the isolated side is electrically monitored and controlled separately from the power that is supplied to the ground-side. More than one DC/DC converter can be used to provide a larger amount of power to the isolated side. The electrical isolation of the components on the isolated side from the ground-side is approximately 5kV.

[0082] The impedance module **20** comprises processing circuitry **52**, interface circuitry **54**, voltage processing circuitry **56** and a current generator **58**. The processing circuitry **52** controls the operation of the impedance module **20**. In particular, the processing circuitry **52** controls parameters related to the generation of current stimulus signals, the measurement of the resulting voltage signals and the analysis of the voltage and current stimulus signals to calculate impedance values for the first and second body parts. The processing circuitry **52** also includes circuitry for communicating with the main module **18**. The voltage processing circuitry **56** processes voltages that are measured by the front-end module **22** at one of the first and second body parts. The voltage processing circuitry **56** includes circuitry for filtering noise from the measured voltages and amplifying the measured voltages. The current generator **58** includes circuitry for generating the stimulus currents for injection to at least one of the first and second body parts. The processing circuitry **52**, the voltage processing circuitry **56** and the current generator **58** are connected by the interface circuitry **54**. It should be understood by those skilled in the art that the term circuitry includes discrete circuit components as well as integrated circuits such as memory chips, data conversion chips (i.e. analog-to-digital converters, etc.) and programmable logic arrays, for example.

[0083] The front-end module **22** includes a multiplexer controller **22a**, a first multiplexer unit **22b** and a second multiplexer unit **22c**. The first multiplexer unit **22b** is connected to the first electrode array **24** and the second multiplexer unit **22c** is connected to the second electrode array **26**. The multiplexer controller **22a** determines which electrodes in the first and second electrode arrays **24** and **26** are used for injecting current into the first and second body parts and which electrodes in the first and second electrode arrays **24** and **26** are used to obtain voltage measurements. The multiplexer controller **22a** provides digital address control to the first and second multiplexer units **22b** and **22c** to select the four connections. The multiplexer controller **22a** is controlled by a processing unit contained within the impedance module **20** or by the computing device **12**.

[0084] For each impedance measurement, four connections are preferably made at a time. For instance, using the first electrode array **24** as an example, two connections are made to current injection electrodes and two connections are made to voltage measurement electrodes. The current injection electrodes are used to inject current into the first body part and to output current from the first body part, respectively. The voltage measurement electrodes are used to measure the voltage that is produced across the first body part tissue by the injected current. By using separate electrode pairs for current injection and voltage measurement, polarization effects at the voltage measurement electrodes are minimized and a more accurate measurement of impedance can be produced. In addition, the series resistance of the signal pathways up to and including the skin does not impact the measurement. Furthermore, the electrodes that are used for current injection and those that are used for voltage measurement can be interchanged to provide more measurement data. To facilitate impedance measurement, the front-end module **22** returns the patient input current and the measured voltage from the patient to the impedance module **20** (as well as the computing device **12** for storage and analysis). The front-end module **22** can also return the common-mode voltage of the measured voltage signal, as well as current-shield and voltage-shield voltages (which are further described below).

[0085] Referring now to Figure 2, shown therein is a block diagram of an embodiment of the impedance module **20**. The processing circuitry **52** of the impedance module **20** includes a UART (universal asynchronous receiver/transmitter) **60**, a complex programmable logic device (CPLD) **61**, a processing unit **62** and a memory unit **64**. The interface circuitry **54** includes a bus **66**, an analog to digital converter (ADC) **68**, and a digital to analog converter (DAC) **70**. The voltage processing circuitry **56** includes a signal conditioning unit **72** and a programmable gain unit **74**.

[0086] The UART **60** converts serial signals received from the computing device **12** to memory-mapped parallel signals. The UART **60** uses the TTL or a RS232 serial communication standard. The processing unit **62**

runs a data acquisition software module (i.e. the DAF module described in more detail below). The processing unit **62** obtains the data signals from the UART **60** via the bus **66**. The memory unit **64** is used to store the DAF module so that the instruction code is not lost when there is no power provided to the medical diagnostic system **10**. The memory unit **64** also stores calibration information that is used to calibrate raw calculated impedances. In one embodiment, a TI 5400 digital signal processor is used as the processing unit **62** and a FLASH ROM is used as the memory unit **64**.

[0087] The CPLD **61** is programmed to include control registers to determine the selection of peripherals, memory mapped registers for controlling other peripherals (such as multiplexers) and memory mapped registers for controlling the communication between the processing unit **62** and the computing device **12**.

[0088] The processing unit **62** includes a calculator module **62a**, for calculating impedance values from measured voltage signals and injected current signals, and a calibrator module **62b** for calibrating the measured impedance values. The processing unit **62** includes on chip random access memory (RAM) and controls the ADC **68**, the DAC **70**, the programmable gain unit **74**, and the current generator **58**. The function of the processing unit **62** can be controlled by software instructions from the medical diagnostic program **16** as well as the DAF module. In this manner, the performance of the medical diagnostic system **10** can be easily adjusted.

[0089] The memory unit **64** stores the DAF module which is loaded into the on chip RAM of the processing unit **62** upon reset and power-up. The memory unit **64** also stores software that allows the processing unit **62** to poll the UART **60** for new communications data, and to use the new data to direct the action of the processing unit **62**. The DAF module allows the processing unit **62** to constantly monitor all signals while polling the UART **60**, and to change the following features based on information received from the computing device **12**: the shape, magnitude and frequency of the generated current waveform, data sampling parameters, whether to return calibrated or

uncalibrated data to the medical diagnostic program **16**, and the gain of the programmable gain unit **74**.

[0090] The processing unit **62** can vary a number of parameters related to data acquisition. For example, the processing unit **62** can adjust the inter sample delay as well as the number of samples per cycle in order to achieve stimulation and measurement at a wide variety of frequencies. The processing unit **62** can also adjust the number of cycles during which data samples are recorded. This minimizes the effect of noise on the measured voltage signals since the signal to noise ratio of a particular spectral range is proportional to the data acquisition time, as is commonly known to those of skilled in the art. In addition, the processing unit **62** can acquire data for performing a second impedance measurement at saturation to calculate a more precise impedance phase.

[0091] The processing unit **62** can also employ under-sampling analog to digital (A/D) and digital-to-analog (D/A) conversion techniques to record results with more equivalent samples/cycle by employing longer acquisition times. Relevant to under-sampled A/D conversion is the Nyquist criterion, which states that Fs>2*Fb where Fs is the sampling rate and Fb is the bandwidth of the signal in question. When measuring sinusoids, the bandwidth is zero. The only sampling rates that cannot be used to record a sinusoid are integer divisions of the frequency of the sinusoid, i.e. a 10 Hz sinusoid cannot be sampled at a rate of 5 Hz or 2.5 Hz but can be sampled at a rate of 1.76 Hz for example. If an integer division of the frequency of the sinusoid is used, sampling at the same place occurs each period leading to a DC result. Otherwise, missing samples are picked up from the next successive periods of the signal to make a single period of the sampled signal. By not sampling at the same corresponding place every time, every sample yields refining information about the sinusoidal signal.

[0092] In the special case where the sampling rate is given by Fs = Fsinusoid*K(a/a+1), where K is a constant ratio related to the gain values that are provided by the programmable gain unit **74** and a is some positive integer,

a signal is acquired that looks exactly like the desired signal to be measured with a sampling rate of K*a samples per cycle. But, in fact, each sample is recorded from a different period. Such results are best obtained with accurate sample timing and a band limited signal. A similar method can be used for D/A conversion. However, a band pass filter instead of the low pass filter is employed resulting in a harmonic generated at the frequency |Fsinusoid-Fs|.

[0093] The ADC **68** and the DAC **70** are connected to the bus **66**. The ADC **68** and DAC **70** can be any suitable data converters that provide sufficient resolution and number of channels. For example, the ADC **68** can have 12 bit resolution and 8 channels while the DAC **70** can have 10 bit resolution and 8 channels. The ADC **68** receives both AC and DC diagnostic signals from a multiplexer (the diagnostic signal selector) in the front-end module **22** and relays the diagnostic signals to the processing unit **62** via the bus **66**. Diagnostic signals related to current levels can be measured through current measuring resistors. The DC diagnostic signals include +5V and –5V power supply voltages, the ADC **68** reference signal voltage, one-half of the ADC **68** reference signal voltage, and the DC offset voltage of the output signal from the DAC **70**. The AC diagnostic signals include driven-shield voltages for all current and voltage measuring electrodes, and voltage and current output signal offsets from their nominal values.

[0094] The current generator **58** is connected to the ADC **68** and the DAC **70**. The current generator **58** generates current signals in response to control signals that are received from the processing unit **62** via the bus **66** and the DAC **70**. The rate at which the control signals are generated by the DAC **70** can be kept relatively low to reduce the power expended. The current generator **58** is also connected to the front-end module **22** to provide a current signal (I+) and a complementary current signal (I-). The current generator **58** is also connected to the ADC **68** to provide signals indicative of the operation of the current generator **76** as well as the complementary current signal I- so that the processing unit **62** can calculate the impedance from corresponding voltage measurements.

[0095] The current generator **58** includes a variable capacitor that controls the phase shift of the complementary current signal (I-), and large series resistors and series capacitors through which the current (I+) and complementary current (I-) signals pass to ensure that variations in load resistance do not significantly affect the operating point of the medical diagnostic system **10**. Adjustment of the variable capacitor assures that the current (I+) and complementary current (I-) signals are as balanced as possible to reduce the common mode signal between them. The series resistors and series capacitors also protect the patient from large fault currents. The current generator **76** also includes optional circuitry for generating current shield voltages for both the current (I+) and complementary current (I-) signals, which are the voltages on the current leads themselves reproduced and multiplied by a set factor between 0.5 and 2 using an amplifier. The complementary current signal I- is measured in amplitude and phase and used for the impedance calculation. The current generator **58** is discussed in more detail below.

[0096] The signal conditioning unit **72** is connected to the front-end module **22** and the programmable gain unit **74**. The signal conditioning unit **72** includes circuitry for providing differential voltage pre-amplification, common-mode rejection, common-mode measurement and filtering. The signal conditioning unit **72** includes a passive common-mode rejection network into which the measured differential voltage signals V+ and V- are supplied. Shield voltages may be generated, as an option, from the returning voltage signals using circuitry similar to that used to generate the shield signals for the current and complementary current signals I+ and I- The signal conditioning unit **72** is described in more detail below.

[0097] The signal conditioning unit **72** receives the measured voltage signals from the front end module **22** and processes the measured voltage signals, as described above, to produce processed measured voltage signals. The signal conditioning unit **72** then sends the processed measured voltage signals to the programmable gain unit **74**. The programmable gain unit **74**

amplifies the processed measured voltage signals to produce amplified measured voltage signals which are sent to the processing unit **62** via the ADC **68** and the bus **66**.

[0098] The programmable gain unit **74** provides multiple levels of gains which are multiples of one another. In this particular embodiment, six levels of gains are provided according to 1, K, K^2, K^3, K^4, and K^5 where K is a constant. This range of gains allows for small processed measured voltage signals to occupy as many bits of the ADC **68** as possible in order to reduce magnitude dependant noise. A programmable gain amplification algorithm is used in conjunction with the programmable gain unit **74** to actively adjust the gain to provide maximum gain while not saturating the output voltage of the programmable gain unit **74**. Saturation can be determined by analysis of the second and third harmonics of the amplified measured voltage signals.

[0099] Referring now to Figure 3a, shown therein is a block diagram of an embodiment **100** of the current generator **58**. The current generator **100** includes a single-ended to differential conversion unit **110**, a first current generation module **112**, a second current generation module **114**, a current measurement unit **116**, a first output impedance network **118**, a second output impedance network **120**, a first current shield signal generator **122** and a second current shield signal generator **124**. A single-ended current control voltage signal **126** from the DAC **70** is provided single-endedly to differential conversion unit **110** which, in response, generates a differential current control voltage signal **128**. Accordingly, the current generator **76** is driven by the output of the DAC **70** which can send arbitrary current waveforms of any frequency.

[00100] The single-ended current control voltage signal **126** is at the same frequency as the generated current and complementary current signals I+ and I- and is preferably a sinusoid. The frequency is chosen to be suitable for bio-impedance applications such as 50 kHz. However, there is an extended range of frequencies that may be used For example, the frequency may be selected according to (50 kHz)•K^n, where K is a constant ratio and is

not necessarily an integer, such as 1.7 for example, and n is any positive or negative integer.

[00101] The first current generation module **112** receives the differential current control voltage signal **128** and generates an internal current signal $I+_{int}$. The internal current signal $I+_{int}$ is provided to the second current generation module **114** which generates an internal complementary current signal $I-_{int}$ which is 180 degrees out of phase with the internal current signal $I+_{int}$. The internal complementary current signal $I-_{int}$ is measured by the current measuring unit **116** and used as a diagnostic signal for the medical diagnostic program **16** to monitor the operation of the current generator **76**. The current measuring unit **116** may include any current measuring circuitry as is commonly known to those skilled in the art. In the embodiment shown in Figure 4a, the current measuring unit **116** includes a current measuring resistor R_{cm}, through which the internal complementary current $I-_{int}$ generates a voltage that is measured by a common-mode rejecting instrumentation amplifier **130** (other amplifier arrangements may be used).

[00102] The internal current signal $I+_{int}$ and the complementary internal current signal $I-_{int}$ are sent to the first and second impedance networks **118** and **120** respectively which generate current signal I+ and complementary current signal I-. The first and second impedance networks **118** and **120** preferably have high-output impedance. Consequently, the current and complimentary current signals I+ and I- are each load-independent currents. The first and second impedance networks **118** and **120** are also used to limit the magnitude of the internal current signal $I+_{int}$ and the complementary internal current signal $I-_{int}$ in order to protect the patient. Accordingly, the current signal I+ and complementary current signal I- are limited magnitude versions of the internal current signal $I+_{int}$ and the complementary internal current signal $I-_{int}$ respectively.

[00103] The voltage levels of the current signal I+ and complementary current signal I- are then provided to the first and second current shield generators **122** and **124**, respectively, to generate the current shield signal

I+S and the complementary current shield signal I-S. The current shield generators **122** and **124** are optional. However, the current shield generators **122** and **124** provide noise and capacitance load reduction in the generated stimulus currents. The current shield generators **122** and **124** can be driven with the same signal that they are shielding or with an amplified or attenuated version of the signal that they are shielding. However, driving a current shield generator with a slightly amplified version of the signal to be shielded allows capacitance above that associated with the measurement leads to be cancelled out. The current shield generators **122** and **124** provide negative capacitance to cancel out the capacitance that is associated with long measurement leads and other stray elements. The current shield signal I+S and the complementary current shield signal I-S are amplitude-adjusted versions of the voltage levels on the leads of the current signal I+ and complementary current signal I- respectively.

[00104] The connection cable between the impedance module **20** and the front-end module **22** comprises four wires. Two of the wires are used for transmitting the current signal I+ and complementary current signal I- to the multiplexer controller **52**. The remaining two wires are used for transmitting the current shield signal I+S and the complementary current shield signal I-S. The orientation of the four wires is such that the current shield signal I+S and the complementary current shield signal I-S are used to shield the current and complementary current signals I+ and I- from noise as well as stray capacitance. This is important since the connection cable between the impedance module **20** and the front-end module **22** can be quite long in some cases.

[00105] The current generator **100** generates the current and complementary current signals I+ and I- and provides these signals to the patient as a differential current. This allows a virtual ground to exist between the two current injection points and the voltage measurement points (the current injection points and measurement points correspond to electrodes). This is beneficial for providing a differential voltage measurement in which

firstly, there is less common-mode voltage between the two voltage measurements and secondly, the input range of the voltage processing circuitry **56** can be made smaller since the measured voltages are centered about ground and a differential voltage measurement is made. A set of controlled impedances are used in the I+ and I- signal pathways of the current generator **100** so that sources of the current and complementary current signals I+ and I- are balanced with respect to one another. In this way, a virtual ground (or zero voltage) appears between the current and complementary current signals I- and I+. Furthermore, the voltages related to the current signals I+ and I- vary depending on the load in order to maintain a constant current.

[00106] Referring now to Figure 3b, shown therein is a circuit schematic for an exemplary embodiment **110'** of the single-ended to differential conversion unit **110**. The single-ended to differential conversion unit **110'** comprises a network of resistors **R5**, **R6** and **R7** and a capacitor **C9**. One end of the resistor **R5** is tied to ground and one end of the resistor **R7** is connected to the single-ended current control voltage signal **126**. The other ends of the resistors **R5** and **R7** are connected across the resistor **R6**. The capacitor **C9** is in parallel with the resistor **R6**. The resistors **R5**, **R6** and **R7** act as a voltage divider and the resistor **R6** and the capacitor **C9** act as a filter.

[00107] Referring now to Figure 3c, shown therein is a circuit schematic for an exemplary embodiment **112'** of the first current generation unit **112**. The first current generation unit **112'** includes a first gain stage **132** and a current generation stage **134**. The first gain stage **132** and the first current generation stage **134** collectively employ instrumentation amplifiers **U2** and **U4** and operational amplifiers **U3A**, **U5A** and **U5B**. Each of the operational amplifiers used in the circuitry shown in Figures 3b-4g are Burr-Brown OPA2743 operational amplifiers. Each of the instrumentation amplifiers used in the circuitry shown in Figures 3b-4g are Burr-Brown INA128 instrumentation amplifiers. Other suitable operational and instrumentation

amplifiers may be used. However, the Burr-Brown instrumentation amplifiers are low power, general-purpose instrumentation amplifiers that offer excellent accuracy. The resistor connected between the +/- gain inputs of the Burr-Brown instrumentation amplifiers set the gain and the input R of the Burr-Brown instrumentation amplifiers provide a reference level about which the output of the instrumentation amplifiers is centered.

[00108] In addition, in Figures 3b-4g, resistors are generally added in series with the inputs of amplifiers to limit the current that may flow to the leads connected to the patient in the event that the amplifiers' internal circuitry fails.

[00109] The first gain stage **132** comprises an amplification stage **136**, a filter stage **138** and a feedback stage **140**. The first gain stage **132** also includes measurement node **ROM** as shown. The amplification stage **136** comprises the instrumentation amplifier **U2** with a resistor **R8** connected between the +/- gain inputs and the output of the feedback stage **140** providing the reference voltage for the amplifier **U2**. The input of the instrumentation amplifier **U2** is the differential current control voltage signal **128** which the amplifier **U2** amplifies with a low gain factor and converts to a single-ended amplified current control voltage signal **128b**.

[00110] The filter stage **138** comprises a resistor **R9** and a capacitor **C12** connected as a first order low pass filter. The filter stage **138** filters the single-ended amplified current control voltage signal **128b** to remove noise and provide a filtered single-ended current control voltage signal **128c**. Other suitable low-pass filter configurations may be used.

[00111] The filtered single-ended current control voltage signal **128c** is then provided to the feedback stage **140** which processes this signal to provide a reference signal **RU2** for the amplifier **U2**. In this embodiment, the feedback stage comprises an amplifier **U3A** connected with a resistor **R10** and a capacitor **C11** in the integrator configuration. The filtered single-ended current control voltage signal **128c** is integrated to generate the reference signal **RU2**. The integrator configuration of the amplifier **U2** acts as an

averaging filter. Accordingly, the DC or average value of the filtered single-ended current control voltage signal **128c** is inverted and used as the reference signal **RU2** to eliminate any DC bias. The amplifier **U3A** is an operational amplifier.

[00112] The current generation stage **134** comprises a second amplification stage **142** and a second feedback stage **144**. The current generation stage **134** also includes measurement node **OSI** as shown. The second amplification stage **142** comprises an amplifier **U4** with a resistor **R11** connected between the +/- gain inputs. The second feedback stage **144** provides the reference voltage for the amplifier **U4** as well as one of the inputs of the amplifier **U4**. One input of the amplifier **U4** is the filtered single-ended current control voltage signal **128c** and the other input is an integrated version of the a voltage related to the generated internal current signal $I+_{int}$. The amplifier **U4** an instrumentation amplifier that provides a low gain factor. The output current of the amplifier **U4** is the internal current signal $I+_{int}$.

[00113] The second feedback stage **144** comprises a voltage follower **144a** and an integrator **144b**. The voltage follower **144a** includes an operational amplifier **U5A** having a resistor **R13** connected to the non-inverting input of the amplifier **U5A** and the output of the amplifier **U4**. The amplifier **U5A** also has a parallel combination of a resistor **R163** and a capacitor **C109** connected between the output of the amplifier **U5A** and the inverting input of the amplifier **U5A**. The capacitor **C109** and the resistor **R163** eliminate unwanted oscillations in the output of the amplifier **U5A**. The internal current signal $I+_{int}$ passes through the resistor **R13** to create a voltage that is proportional to the internal current signal $I+_{int}$. Assuming that amplifier **U5A** is an ideal op-amp, this voltage appears at the inverting input of amplifier **U5A** and is provided to the reference voltage input **R** of the instrumentation amplifier **U4** and the input of the integrator **144b**. The voltage follower **144a** is used to ensure that the operation of the instrumentation amplifier **U4** is independent of its loading.

[00114] The integrator **144b** comprises an operational amplifier **U5B** with a resistor **R12** and capacitor **C13** connected to the amplifier **U5B** in an integrating configuration. A voltage that is proportional to the internal current signal $I+_{int}$ is integrated by the integrator **144b** and provided to the positive input of the instrumentation amplifier **U4**.

[00115] Referring now to Figure 3d, shown therein is a circuit schematic for an exemplary embodiment **114'** of the second current generation module **114**. The second current generation module **114'** includes a phase adjusting stage **150**, an inverting stage **152** and a current measurement stage **154**. The second current generation module **114'** also includes measurement node **CH1**. The phase adjusting stage **150** adjusts the phase of the internal current signal $I+_{int}$ before it is inputted to the inverting stage **152.** The inverting stage **152** inverts the phase of the internal current signal $I+_{int}$ to generate the internal complementary current signal $I-_{int}$. The current measurement stage **154** is used to measure the internal complementary current signal $I-_{int}$. The measurement of the current signal $I-_{int}$ is used by the processing unit **62** to calculate impedance values.

[00116] The phase adjusting stage **150** can comprise any phase shifting network. In this exemplary embodiment, the phase adjusting stage **150** comprises a variable capacitor **C14** and a resistor **R14** connected in series to provide a phase-lead for the internal current signal $I+_{int}$ and generate the phase-adjusted internal current signal $I+_{int,a}$. The phase adjusting stage **150** is needed to correct for any phase lag that results from the creation of the internal complementary current signal $I-_{int}$ from the internal current signal $I+_{int}$ or from impedance imbalances in the I+ and I- signal pathways.

[00117] The inverting stage **152** comprises an operational amplifier **U3B** with resistors **R16** and **R15** configured in the inverting configuration. The resistor **R16** is connected between the inverting input and output of the amplifier **U3B** and the resistor **R15** is connected to the inverting input of the amplifier **U3B**. The negative input of the amplifier **U3B** receives the phase-adjusted internal current signal $I+_{int,a}$ and provides a phase shift of 180•, by

applying a gain of –1, thus generating the internal complementary current signal $I-_{int}$.

[00118] The current measurement stage **154** comprises an instrumentation amplifier **U6** and resistors **R18**, **R31**, and **R32**. The resistor **R31** is connected between the G-/G+ inputs of the amplifier **U6**. The amplifier **U6** provides a low gain factor of approximately 2. The amplifier **U6** is used to measure the current in the I- signal pathway and provide this current to the processing unit **62** via the ADC **68**. Accordingly, the voltage **RM** that provides a voltage reference for the amplifier **U6** is the center voltage of the input voltage range of the ADC **68** to ensure that the signal measured at node **CH1** is not clipped when being converted by the ADC **68**. The measured current refers directly to the amount that has been sent to the load.

[00119] Referring now to Figure 3e, shown therein is a circuit schematic for an exemplary embodiment of an output impedance network **118'** that can be used for both the first and second output impedance networks **118** and **120**. The output impedance network **118'** receives one of the internal current signals ($I+_{int}$ or $I-_{int}$) and respectively generates the current signal I+ or the complementary current signal I-. The output impedance network **118'** includes a series combination of resistors **R17** and **R19** with capacitor **C15** and a resistor **R20** shunted to ground. The resistors **R17** and **R19** limit the current that is provided to the patient for safety reasons. Both resistors **R17** and **R19** have to fail in order for a large current to be sent to the patient. The capacitor **C15** removes the DC current that is sent to the patient. The resistor **R20** provides a DC path to ground so that the voltage on the I+/I- signal pathway does not increase too much as well as providing a DC path to ground for amplification circuitry in the current shield generators **122** and **124**.

[00120] Referring now to Figure 3f, shown therein is a circuit schematic for an exemplary embodiment of a current shield generator **122'** that can be used for both the first and second current shield generators **122** and **124**. The current shield generator **122'** comprises an operational amplifier **U7B** that is in a voltage follower configuration. Resistors **R27** and **R28** are connected to the

non-inverting and inverting inputs of the amplifier **U7B**. A capacitor **C105** is connected between the output and inverting input of the amplifier **U7B**. Resistors **R159** and **R30** are connected in series at the output of the amplifier **U7B**. A variable resistor **R29** is connected from the inverting input of the amplifier **U7B** to between the series resistors **R159** and **R30**. The resistance of thé resistor **R29** determines the gain of the amplifier **U7B** (when the resistance of the resistor **R29** is zero, the gain of the amplifier **U7B** is 1). The gain of the amplifier **U7B** provides flexibility in allowing the current shield generator **122'** to generate a negative capacitance to cancel out the capacitance that occurs in the connection cable between the impedance module **20** and the front-end module **22** as well as capacitance that occurs in circuitry (such as the multiplexers in the front-end module **22**) that is downstream from the current generator **100**. Generally, the gain of the amplifier **U7B** is in the range of 1.0 to 1.5. Care must be taken in not choosing a high gain since this may lead to the current shield generator **122'** providing too much negative capacitance which will lead to oscillations.

[00121] The output of the current shield generator **122'** is taken from the external node of resistor **R30** and a capacitor **C103** is shunted to ground at the external node of resistor **R30**. The resistor **R158** and the capacitor **C105** eliminate unwanted oscillations from the output of the amplifier **U7B** and provide a path to ground for very high frequency signals coupled externally to the shield. The resistor **R22** is used for protection to the patient in the event that the input resistance of the amplifier **U7B** degrades. The resistor **R24** along with the capacitor **C102** provide low-pass filtering. As previously mentioned, these current shield generators are optional.

[00122] Referring now to Figures 3g-1 and 3g-2, shown therein is a circuit schematic showing all of the exemplary embodiments for the sub-blocks of the current generator **76**. Additional elements have been added at the output of the first and second impedance networks **122'** and **124'** prior to the connection nodes for the current and complementary current signal I+ and I-. In particular, a capacitor **C17**, shunted to ground, and in parallel with a

ferrite bead **L3** has been added in the I+ signal path and a capacitor **C18**, shunted to ground, and in parallel with a ferrite bead **L4** has been added in the I- signal path. The ferrite beads **L3** and **L4** are used to remove unwanted high-frequency signals/noise from the I+ and I- signal paths. An example for the dimension of the ferrite beads that can be used is a length of 0.2 inches and a diameter of 0.1 inches. The capacitors **C17** and **C18**, along with resistors **R19** and **R25**, respectively, provide low-pass filtering. For the exemplary embodiment shown in Figures 4g-1 and 4g-2, an example of values for the resistors and capacitors that can be used are given in Table 1-1. Relationships that should preferably be maintained between particular components are shown in Table 1-2.

Table 1-1: Exemplary component values used in current generator

R5: 4.75 kΩ	**R14**: 10 kΩ	**R23**: variable	**R32**: 100 Ω	**C15**: 10 nF
R6: 1kΩ	**R15**: 10 kΩ	**R24**: 100 Ω	**R158**: 100 Ω	**C16**: 10 nF
R7: 4.75 kΩ	**R16**: 10 kΩ	**R25**: 7.5 kΩ	**R159**: 100 Ω	**C17**: 100 pF
R8: 20 kΩ	**R17**: 1 kΩ	**R26**: 1 MΩ	**R163**: 100Ω	**C18**: 100 pF
R9: 1 kΩ	**R18**: 1 kΩ	**R27**: 100 kΩ	**C9**: 1 nF	**C102**: 100 pF
R10: 100 kΩ	**R19**: 7.5 kΩ	**R28**: 100 kΩ	**C11**: 4.7 nF	**C103**: 100 pF
R11: 10 MΩ	**R20**: 1 MΩ	**R29**: variable	**C12**: 470 pF	**C104**: 10 pF
R12: 100 kΩ	**R21**: 100 kΩ	**R30** 100 Ω	**C13**: 4.7 nF	**C105**: 10 pF
R13: 1 kΩ	**R22**: 100 kΩ	**R31**: 50 kΩ	**C14**: 5-40 pF	**C109**: 10 pF

Table 1-2: Component relationships in current generator

R5 = R7	**R21 = R27** (≥ 10 kΩ)	**R158 = R159**
R15 = R16	**R22 = R28** (≤100 kΩ)	**C15 = C16**
R17 = R18	**R23 = R29** (≥ 0, ≤1.2***R22**)	**C17 = C18** (≤100 pF)
R19 = R25	**R24 = R30**	**C102 = C103** (≤100 pF)
R20 = R26 (≥ R19)	**R45 = R46**	

[00123] Referring now to Figure 4a, shown therein is a block diagram of the voltage processing modules of the impedance module **20**. In particular, the signal conditioning unit **72** is implemented by a first voltage shield generator **160**, a second voltage shield generator **162**, a differential input network **164**, and a differential voltage amplifier **166**. The programmable gain

unit **74** is implemented by a programmable gain amplifier **168**, and an output stage **170**.

[00124] A measured differential voltage signal **172** consists of the measured voltage signals V+ and V- which are each provided by an electrode in at least one of the first and second electrode arrays **24** and **26**. The differential input network **164** processes the measured differential voltage signal **172** by filtering and rejecting common-mode voltages to generate a processed differential voltage signal **174**. The differential voltage amplifier **166** receives the processed differential voltage signal **174**, and amplifies this signal as well as providing a differential to single-ended conversion to generate a single-ended measured voltage signal **176**. The programmable gain amplifier **168** amplifies the single-ended voltage signal **176** by applying a variable gain factor to generate an amplified single-ended measured voltage signal **178**. The magnitude of the variable gain factor is chosen so that the magnitude of the amplified single-ended measured voltage signal **178** is adjusted to fully occupy the input range of the ADC **68**. The output stage **170** then processes the amplified single-ended voltage signal **178** by shifting the DC level of the signal **178** to generate output signal **179**. The output stage **170** ensures that the output signal **179** is centered within the input range of the ADC **68** so that the signal **179** can be sampled by the ADC **68** without being clipped.

[00125] The first voltage shield generator **160** and the second voltage shield generator **162** operate on an internal version of the measured differential voltage signal **172** to generate voltage shield signals V+S and V-S for the measured voltage signals V+ and V- respectively. The voltage shield signal V+S and V-S are fed back to the connection cable between the impedance module **20** and the front-end module **22** to reduce the effects of stray capacitance and other noise on the measured differential signals V+ and V- as was done previously for the current and complementary current signals I+ and I-. Accordingly, the current shield generator **122'** (see Figure 3f) can be used to implement the first and second voltage shield generators **160** and

162. The first and second voltage shield generators **162** and **164** are optional, however, they increase the fidelity of the measurement process by providing a negative capacitance to cancel out stray capacitance in the connection cable between the impedance module **20** and the front-end module **22** as well as capacitance from electronic components that are upstream from the voltage processing circuitry **56**.

[00126] Referring now to Figure 4b, shown therein is a circuit schematic for an exemplary embodiment **164'** of the differential input network **164**. The differential input network **164'** includes a first filtering stage **180**, a common-mode measurement stage **182**, a common-mode rejection stage **184** and a second filter stage **186**. The first filter stage **180** comprises ferrite beads **L5** and **L6** which are followed respectively by capacitors **C21** and **C22** shunted to ground. The ferrite beads **L5** and **L6** are used to remove high-frequency noise from the measured voltage signals V+ and V- respectively. An example for the dimension of the ferrite beads that can be used is a length of 0.2 inches and a diameter of 0.1 inches. The capacitors **C21** and **C22** also filter out high-frequency noise. The first filter stage **180** provides a first filtered measured signals $V+_f$ and $V-_f$.

[00127] The common-mode measurement stage **182** includes a series connection of resistors **R164** and **R165** connected in parallel with the signal paths for the first filtered measured voltage signals $V+_{f1}$ and $V-_{f1}$. The node between the resistors **R164** and **R165** provides a measurement node **CM** for measuring a voltage signal that is directly proportional to the common mode voltage of the first filtered measured signal $V+_{f1}$ and $V-_{f1}$. The measured common-mode voltage is monitored by the processing unit **62** and the medical diagnostic program **16**. The measured common-mode voltage is used by the processing unit **62** to correct the calculated impedance values since the common-mode voltage is not entirely removed from the measured voltages by the voltage processing circuitry **56**.

[00128] The common-mode rejection stage **184** includes a parallel connection of a capacitor **C23** and along with series-connected resistors **R41**

and **R42**. The resistors **R41** and **R42** are used to provide a ground reference at the inputs and a current path to ground for the bias currents of the voltage shield generators **160** and **162**. The capacitor **C23** is used to filter out the high-frequency difference-mode components of the first filtered measured voltage signals $V+_{f1}$ and $V-_{f1}$ to produce second filtered measured voltage signals $V+_{f2}$ and $V-_{f2}$. The upper node where the capacitor **C23** is connected to the V+ signal path is used to provide an input voltage for the first voltage shield generator **160** and the lower node where the capacitor **C23** is connected to the V- signal path is used to provide an input voltage for the second voltage shield generator **162**.

[00129] The second filtering stage **186** receives the second filtered measured voltage signals $V+_{f2}$ and $V-_{f2}$ and performs low-pass filtering on these signals to generate a third measured voltage signal which corresponds to the processed differential voltage signal **174**. The second filtering stage **186** begins with a series connection of capacitor **C24** and resistor **R45** in the V+ signal path and a series connection of capacitor **C25** and resistor **R46** in the V- signal path. A series connection of resistors **R43** and **R44** is connected across the V+ signal path (between the capacitor **C24** and the resistor **R45**) and the V- signal path (between the capacitor **C25** and the resistor **R46**). The node between the resistors **R43** and **R44** is connected to ground. In the V+ signal path, a capacitor **C26** is shunted to ground and connected to the other node of resistor **R45**. Likewise, in the V- signal path, a capacitor **C28** is shunted to ground and connected to the other node of resistor **R46**. A capacitor **C27** is connected between the capacitors **C26** and **C28**.

[00130] The capacitors **C24** and **C25** remove the DC components in the measured voltage signals $V+_{f2}$ and $V-_{f2}$. The resistors **R43** and **R44** provide a DC path to ground for the differential voltage amplifier **166**. The resistor **R45** and the capacitor **C26** provide low-pass filtering in the V+ signal path. Likewise, the resistor **R46** and the capacitor **C28** provide low-pass filtering in the V- signal path. The capacitor **C27** reinforces coupling of noise that is common to both the V+ and V- signal paths and filters differential noise,

thereby restricting the amount by which the common-mode signals are converted to difference-mode signals by the ground-connected filter capacitors.

[00131] Referring now to Figure 4c, shown therein is a circuit schematic for an exemplary embodiment **166'** of the differential voltage amplifier **166**. The differential voltage amplifier **166'** includes an amplification stage **190**, a feedback stage **192** and a filter stage **192**. The amplification stage **190** includes an instrumentation amplifier **U9** with a high common-mode rejection ratio. The amplifier **U9** amplifies the processed differential voltage signal **174** and generates a single-ended measured voltage signal **Vs**. The amplifier **U9** has resistor **R49**connected across the gain inputs G+/G-. The amplifier **U9** also has input resistors **R47** and **R48** connected to the inverting and non-inverting inputs respectively for limiting the input current to the amplifier **U9**.

[00132] The feedback stage **192** includes an operational amplifier **U10B** which has the non-inverting input tied to ground, a feedback capacitor **C30** connected between the inverting terminal and the output terminal and a resistor **R54** connected to the inverting input. Accordingly, the amplifier **U10B** is configured in an integrator configuration. The resistor **R54** is also connected to an internal node within the programmable gain amplifier **168** to provide an indication of the amplified single-ended measured voltage signal **178**. This signal is integrated by the amplifier **U10B** and used as the reference input to the amplifier **U9**. In this fashion, the amplifier **U10B** can track changes in the DC level of the amplified single-ended measured voltage signal **178** and adjust the output signal **Vs** to ensure that this signal is centered about ground. A measurement node **OSV** is connected to the output of the amplifier **U10B** to monitor the performance of the amplifier **U10B**.

[00133] The filter stage **192** receives the single-ended measured voltage signal **Vs** and filters this signal to generate the single-ended measured voltage signal **176**. The filter stage **192** is a single-order low-pass filter network comprising a series connected resistor **R50** and a capacitor **C29** shunted to ground. Other low-pass filter networks may also be used, however

care must be taken with higher-order filter networks since they may present an increasingly indefinite phase lag to the measured voltages.

[00134] Referring now to Figure 4d, shown therein is a circuit schematic for an exemplary embodiment **168'** of the programmable gain amplifier **168**. The programmable gain amplifier **168'** includes an amplifier stage **200**, a variable resistance stage **202** and a filter stage **204**. The amplifier stage **200** includes an operational amplifier **U10A** configured as a voltage follower. The non-inverting input of the amplifier **U10A** receives the single-ended measured voltage signal **176** and the inverting input receives feedback from the output of the amplifier **U10A** via a capacitor **C108**. The output terminal of the amplifier **U10A** is connected to a first node of series resistor **162**. The inverting terminal of the amplifier **U10A** is also connected to the variable resistance stage **202** so that the amplifier **U10A** can provide a variable amount of gain to the single-ended measured voltage signal **176**. The capacitor **C108** and the resistor **R162** eliminate unwanted oscillations from the output of the amplifier **U10A**.

[00135] The gain of the amplifier **U10A** is determined by the variable resistance stage **202**. The variable resistance stage **202** includes a plurality of resistors **R55**, **R56**, **R57**, **R58**, **R59** and **R60** with different resistance values connected to a multiplexer **U12**. The input of the multiplexer **U12** is connected to the inverting input of the amplifier **U10A** and one of the eight output paths of the multiplexer **U12** (i.e. outputs X0, X1, X2, X3, X4, X5, X6 or X7) is connected to the second node of the resistor **R162** through a variety of combinations of the resistors **R55**, **R56**, **R57**, **R58**, **R59** and **R60**. The selection inputs of the multiplexer **U12** (inputs A, B, C) are connected to control signals provided by the processing unit **62**. The processing unit **62** selects one of the eight output paths of the multiplexer **U12** based on the desired gain for the amplifier **U10A**. The desired output path is selected in accordance with a variable gain algorithm that is implemented by the processing unit **62**.

[00136] The paths associated with outputs X1, X2, X3, X4, X5, X6 or X7 provides an equivalent resistor Req that is the parallel combination of two combination resistors RC1 and RC2. The combination resistors RC1 and RC2 are formed from a series combination of resistors selected from **R55**, **R56**, **R57**, **R58**, **R59** and **R60**. For instance the output path associated with output X0 results in combination resistor RC2 equal to the series combination of resistors **R55**, **R56**, **R57**, **R58**, **R59** and **R60** and combination RC1 equal to 0 Ω. The output path associated with output X1 results in combination resistor RC2 equal to the series combination of resistors **R56**, **R57**, **R58**, **R59** and **R60** and combination RC1 equal to resistor **R55**. The output path associated with output X2 results in combination resistor RC2 equal to the series combination of resistors **R57**, **R58**, **R59** and **R60** and combination RC1 equal to the series combination of resistors **R55** and **R56**. The output path associated with output X3 results in combination resistor RC2 equal to the series combination of resistors **R58**, **R59** and **R60** and combination RC1 equal to the series combination of resistors **R55**, **R56**, and **R57**. The output path associated with output X4 results in combination resistor RC2 equal to the series combination of resistors **R59** and **R60** and combination RC1 equal to the series combination of resistors **R55**, **R56**, **R57** and **R58**. The output path associated with outputs X5, X6 or X7 results in combination resistor RC2 equal to resistor **R60** and combination RC1 equal to the series combination of resistors **R55**, **R56**, **R57**, **R58** and **R59**.

[00137] The combination resistor RC1 is effectively connected between the inverting input of the amplifier **U10A** and the second node of resistor **R162** and the combination resistor RC2 is effectively connected between the inverting terminal of the amplifier **U10A** and ground. The values of the combination resistors RC1 and RC2 are selected to ensure that the gains provided by the amplifier **U10A** is in accordance with $G_N=G_1*K^N$ as well as for calibration.

[00138] The filter stage **204** receives the output of the amplifier **U10A** and filters this signal to provide the amplified single-ended measured voltage

signal **178**. The filter stage **204** is a first order low pass filter network which includes a series resistor **R51** and a capacitor **C31** shunted to ground. However, the filter stage **204** can be any low-pass filter stage.

[00139] Referring now to Figure 4e, shown therein is a circuit schematic for an exemplary embodiment **170'** of the output stage **170**. The output stage **170'** includes an instrumentation amplifier **U11** configured for unity gain. A resistor **R53** is connected to the output of the amplifier **U11**. The output signal **179** is provided to the ADC **68**. Accordingly, the reference input **RM** of the amplifier **U11** is provided by the reference of the ADC **68** to ensure that the output signal **179** is centered about the mid-point of the input range of the ADC **68** so that the ADC **68** can sample the output signal **179** without clipping.

[00140] Referring now to Figures 4f-1 and 4f-2, shown therein is a circuit schematic showing all of the exemplary embodiments of the components of the voltage processing modules of the impedance module **20**. For the exemplary embodiment shown in Figures 5f-1 and 5f-2, an example of the values of the resistors and capacitors that can be used are given in Table 2-1. Relationships that should preferably be maintained between particular components are shown in Table 2-2.

Table 2-1: Exemplary component values used in voltage measurement

R33: 100 Ω	**R43**: 1 MΩ	**R52**: 10 MΩ	**R161**: 100 Ω	**C25**: 10 nF
R34: variable	**R44**: 1 MΩ	**R53**: 100 Ω	**R162**: 100 Ω	**C26**: 10 pF
R35: 100 kΩ	**R45**: 10 kΩ	**R54**: 100 kΩ	**R164**: 50k Ω	**C27**: 47 pF
R36: 100 kΩ	**R46**: 10 kΩ	**R55**: 4.12 kΩ	**R165**: 50k Ω	**C28**: 10 pF
R37: 100 Ω	**R47**: 100 kΩ	**R56**: 2.43 kΩ	**C19** : 100 pF	**C29**: 100 pF
R38: variable	**R48**: 100 kΩ	**R57**: 1.43 kΩ	**C20**: 100 pF	**C30**: 4.7 nF
R39: 100 kΩ	**R49**: 11kΩ	**R58**: 845 Ω	**C21**: 10 pF	**C31**: 100 pF
R40: 100 kΩ	**R50**: 1 kΩ	**R59**: 499 Ω	**C22**: 10 pF	**C106**: 10 pF
R41: 1 MΩ	**R51**: 1 kΩ	**R60**: 698 Ω	**C23**: 10 pF	**C107**: 10 pF
R42: 1 MΩ	**R42**: 1 MΩ	**R160**: 100 Ω	**C24**: 10 nF	**C108**: 10 pF

Table 2-2: Component relationships in voltage measurement

R33 = R37	**R47 = R48** (≤100 kΩ)	**R164 = R165**
R34 = R38 (≤1.2 Ω)	**R55=**$K^4(K-1)$***R60**	**C19 = C20**
R35 = R39 (≤100 kΩ)	**R56=**$K^3(K-1)$***R60**	**C21 = C22** (≤ **C23**)
R36 = R40 (≥10 kΩ)	**R57=**$K^2(K-1)$***R60**	**C24 = C25**
R41 = R42	**R58=**$K(K-1)$***R60**	**C26 = C28** (≤ **C27**)
R43 = R44	**R59=**$(K-1)$***R60**	
R45 = R46	**R160 = R161**	

[00141] The design of the current generator **58**, the signal conditioning unit **72** and the programmable gain unit **74** shown herein allow the impedance module **20** to be attached to the front-end module **22** through a highly parasitic interface as well as configurations that have a high common mode while continuing to measure both magnitude and phase correctly.

[00142] The processing unit **62** includes a calculator module **62a** for converting measured voltages and currents into impedance values. The calculator module **62a** may be implemented in software or hardware. To calculate an impedance value, the calculator module **62a** calculates, at the measurement frequency, the ratio of the magnitude of the measured return voltage and magnitude of the generated current, and the difference between the phase of the measured return voltage and the generated current.

[00143] The processing unit **62**, in conjunction with the calculator module **62a**, may vary the number of samples/cycle and the number of acquisition cycles to maintain a minimum signal to noise ratio. The processing unit **62** may also instruct the ADC **68** to perform under-sampling since the measured signals are sinusoids that ideally have zero bandwidth. High-speed analog-to-digital converters and digital-to-analog converters are power hungry and therefore unsuitable for most biomedical instrumentation applications. Accordingly, under-sampling, which involves using a lower sampling rate, results in lower power consumption.

[00144] The processing unit **62** also includes the calibrator module **62b** for correcting calculated impedances for systematic imperfections in the measurement system. The calibrator module **62b** may be implemented in software or hardware. The calibration performed by the calibrator module **62b** allows the impedance module **20** to be connected to a wide variety of interfaces while retaining precision and accuracy in voltage measurement. The calibration process includes two-steps: 1) impedance calibration and 2) common-mode calibration. The sequence of these steps does not matter as long as one always uses the same sequence of steps.

[00145] The common-mode calibration step involves reducing the common-mode in the measured voltage signal. Although, the instrumentation amplifiers used in the signal conditioning unit **72** have a high common-mode rejection ratio, the rejection is not perfect. In addition, as frequencies increase, the common-mode rejection ratio of these amplifiers degrades. Consequently, a common-mode voltage, which generally has a different phase from the impedance phase, remains in the processed measured voltages and prevents the accurate measurement of differential voltage phase. To improve common-mode rejection, the calibrator module **62b** calculates the magnitude and the phase of the measured common-mode signal at the frequency of the current signals I+ and I- (see node **CM** between resistors **R164** and **R165** in the differential input network **164'** shown in Figure 4b). The measured voltage is then corrected with the measured common-mode signal in one of two fashions. The first way to correct the measured voltage signal for common-mode voltage is to use a weighted subtraction of the measured common-mode signal. The second way to correct the measured voltage signal for common-mode voltage is to use a lookup table indexed with the magnitude and phase of the measured common-mode signal. Either of these common-mode calibration schemes can be used.

[00146] In the weighted subtraction common-mode calibration method, the weight used is related to the common-mode rejection ratio of the differential voltage amplifier **166** and the amount of filtering provided by the

common-mode rejection stage **184**. For instance, if the common-mode rejection stage **184** provides 20 dB of attenuation and the common-mode rejection ratio of the differential voltage amplifier **166** is 100 dB, then the weight is –120 dB or 10^{-6}.

[00147] In the second method of common-mode voltage correction, the lookup table can be generated by presenting a variety of known common-mode voltages on a standard measurement load, at the input of the voltage processing circuitry **56** and then measuring the common-mode voltage in the processed measured voltages to obtain complex correction numbers. The lookup table is constructed by using the magnitude and phase of the known common-mode voltages as indices into the lookup table and the entries in the lookup table are the corresponding common-mode calibration values (which are generally complex numbers). The common-mode calibration value is subtracted from the measured common-mode voltage. If the measured common-mode voltage has a magnitude and phase that falls between the magnitude and phase indices used to create the lookup table, then interpolation can be used to obtain the common-mode calibration value. The interpolation may be linear, logarithmic or polynomial.

[00148] The impedance calibration step involves converting measured complex impedance values to "true" impedance values by reducing systematic errors (due to the measurement circuitry) from the measured voltage values. These errors exist as a result of the reactive and resistive elements in the measurement signal path. In particular, the impedance calibration step reduces the effects of phase shifts and attenuations in all of the amplifiers in the signal conditioning unit **72** and the dependence of these effects on the frequency, load magnitude, and the gain of the programmable gain unit **74**. To facilitate impedance calibration, the impedance calibration step employs the use of a set of multipoint calibration tables. A set of such tables is required since at each gain, at each stimulus frequency and at each load, the systematic errors are different and calibration is required at all possible operating points. The calibration step is done before the medical

diagnostic system **10** is used to obtain impedance measurements. Thereafter, the calibration step can be done periodically to ensure that the calibration tables are up-to-date. The set of calibration tables can be stored in the memory unit **64**. The appropriate calibration table, as determined by the frequency used for the injection current, can then be retrieved from the memory unit **64** as required by the processing unit **62** when calculating impedance values.

[00149] Calibration values for a particular calibration table are generated by keeping the stimulus frequency constant and varying the magnitudes of the calibration impedance and the gain levels provided by the programmable gain unit **74**. The calibration values in a column of the calibration table can be obtained by performing measurements with a constant gain while increasing the magnitude of the calibration impedance. The calibration values in a row of the calibration table can be obtained by performing measurements on a constant calibration impedance while increasing the gain of the programmable gain unit **74**. This measurement process is repeated for different stimulus frequencies. The result is a set of calibration tables with each table corresponding to a particular stimulus frequency.

[00150] While performing the calibration measurements, a common constant ratio K is used to guarantee monotonicity across all gain ranges, and the use of a minimal set of calibration impedances. The constant ratio K preferably has a value that is greater than one and generally less than two. The calibration is performed for gain levels defined by $G_N=G_1*K^N$ where G_1 may be 1 for example. Likewise, the frequencies at which calibration is done is also related by the constant factor K in as defined by $F_N=F_1*K^N$ where the frequency F_1 is 50 kHz for example. Accordingly, the constant ratio K is used to determine the various combinations and values of the resistors **R55**, **R56**, **R57**, **R58**, **R59** and **R60** in the variable resistance stage **202** (see Figure 4d) of the programmable gain amplifier **168** as well as the spacing of the frequency that is used for the current and complementary current I+ and I- (stimulus) injection signals generated by the current generator **58**.

[00151] The result of the constant ratio K is a unique diagnostic calibration table in which, if all system components were ideal, the calibration values in a given row of the calibration table would be K times the calibration values in the row just above the given row and the calibration values in a given column of the calibration table would be K times the calibration values in the column just to the left of the given column. Accordingly, the calibration table can be verified for validity by basing one or more metrics on the self-consistency of the data in the calibration table since the calibration table can be approximately predicted by knowing any single value in it and the factor K. Correspondingly, an enormous amount of data can be extracted from a single calibration table in this way, and errors in calibration (which would certainly cause measurement problems) will be easily identified. Overall, the calibration table provides data on how the system performs at different frequencies while measuring different loads with a certain phase at different gains, and can be used to completely characterize the medical diagnostic system **10** as a whole.

[00152] The impedance calibration step involves connecting a calibration board (not shown) that has a calibration impedance network to either one of the first multiplexer unit **54** or the second multiplexer unit **56** instead of the first and second electrode arrays **24** and **26**. The calibration board may be internal or external to the medical diagnostic system **10**. Alternatively, the calibration board may be connected to the voltage processing circuitry **56** of the impedance module **22** via selection circuitry such as a multiplexer or the like or via connection leads that are manually connected to the different calibration impedances on the calibration board. The calibration network comprises a plurality of resistors and capacitors that are selectively connected in series to form a calibration impedance. The resistance of the calibration resistors are related to one another according to $R_N=R_1*K^N$ where the resistance R_1 can be 10 Ω, for example, and the capacitance of the capacitors are related to one another according to $C_N=C_1*K^N$ where the capacitance C_1 can be 0.1 μF for example.

[00153] The result of using the constant ratio K for the selection of the calibration resistor values and the calibration capacitor values is the optimum reuse of the calibration resistors and the calibration capacitors for calibration at different calibration frequencies. For instance, at a particular operating frequency $F = F_N$, for a calibration impedance consisting of a series combination of a calibration resistor R_N and a calibration capacitor C_N, the phase is $phase_1=\tan^{-1}(R_N*C_N*F_N)$ At an operating frequency $F=F_{N+1}$, the same load has a phase of $phase_2=\tan-1(R_N * C_N *F_{N+1})$. In order for the measured calibration loads to have an identical phase at both frequencies (i.e. $phase_2 = phase_1$), since $F_{N+1}=K* F_N$ the required value of the calibration capacitance is C_N/K. The capacitance value of C_N/K is provided by the capacitor C_{N-1} which exists on the calibration board. Similarly, the value of the calibration capacitor required for a calibration resistor having a resistance value of R_{N+1} when the operating frequency is F_N, is the same calibration capacitor that is required by a calibration resistor having a resistance value of R_N when the operating frequency is F_{N+1}. Accordingly, a small set of calibration resistors and calibration capacitors on the calibration board can span the complete required set of calibration impedances.

[00154] As an example, if 16 calibration elements are used for the calibration network, there can be 12 calibration resistors and 4 calibration capacitors or alternatively 11 calibration resistors and 5 calibration capacitors. Generally, there are more calibration resistors on the calibration board than calibration capacitors because in practice the magnitude range for measured impedance values is larger than the phase range. In this example, there are 12 completely reactive possibilities, 131 purely resistive possibilities and 48 mixed reactive/resistive possibilities.

[00155] In general, the rows of a given calibration table are indexed by the impedance magnitude and the columns of the calibration table are indexed by the gain of the programmable gain unit **168**. When an impedance value is calculated, the frequency of the stimulus current determines which table is used and the gain of the programmable gain unit **168** determines

which column is used to obtain an impedance correction factor from the table. The row of the table is given by the magnitude of the measured impedance. The calculated impedance value is then multiplied by the correction value to obtain a corrected or "true" impedance value. However, if the magnitude of the measured impedance does not correspond with the magnitude of one of the calibration impedances, then interpolation is used on the correction values within the appropriate column of the calibration table to determine a suitable correction value. The interpolation may be linear, exponential or the like.

[00156] Thus far, the generation of the calibration tables have assumed that there are only magnitude variations in the measurement of an impedance value as the gain or frequency used by the impedance module **20** is varied. However, there can also be instances in which there are also phase variations in the measurement of an impedance value as the gain or frequency used by the impedance module **20** is varied. In this case, the calibration tables may be generated such that there is a variation in the calibration impedance. It is assumed that the phase variation is linear and so two calibration tables are generated for each stimulus frequency in which the phase of the calibration impedances is kept constant for each table but there is a phase difference between the calibration impedance for the pair of calibration tables. For instance, one calibration table may be generated based on calibration impedances that have a phase of 0 degrees the other calibration table may be generated based on calibration impedances that have a phase of 10 degrees, for example. In this case, when obtaining the correction factor based on the magnitude and phase of a measured impedance, if the phase does not correspond to one of the phases used to generate the tables at a particular stimulus frequency, then linear interpolation can be used to obtain an appropriate correction value. This interpolation may also include an interpolation on the impedance magnitudes used to generate the calibration tables thus resulting in a interpolation across two dimensions.

[00157] The medical diagnostic software program **16** comprises two software modules: the TAS (Test and Analysis software) and DAS (Data

Acquisition software) modules that operate on the computing device **12**. The TAS module is a graphical user interface that provides an interface to allow a user to initiate impedance testing and view and analyze the resulting impedance values. The DAS module operates in conjunction with the TAS module to set test parameters and obtain test data for analysis and viewing. The TAS module interfaces with the DAF (Data Acquisition Firmware) which resides in the impedance module **20** and directs the activities of the impedance module **20**. The DAS and the DAF modules communicate through the serial interface between the computing device **12** and the medical diagnostic system **10**.

[00158] The DAF module remains in an idle state until commands are received which cause it to act. While idle, the DAF module constantly monitors all system information available to it. The magnitude of each DC voltage supply level as well as the ripple of each DC voltage supply level is available to the DAF module through the ADC **68**. The most recent measurements of these signals is stored in the memory unit **64** and can be accessed through commands sent to the DAF module via the serial link from the computing device **12**. If any of these measurements is outside a pre-defined acceptable range, the next measurement returned to the DAF module will be an error code detailing the problem.

[00159] When the impedance module **20** is first powered-on or reset, the DAF module is loaded into the on-chip memory of the processing unit **62** from the memory unit **64**. The on-chip program memory of the processing unit **62** is compared to that in the memory unit **64** to ensure that this process was completed successfully. Once this is verified, the DAF module verifies all impedance module **20** power levels and initializes the impedance module **20** to perform voltage measurements at a pre-determined frequency such as 50 kHz for example. The initialization at the pre-determined frequency involves downloading a calibration table from the memory unit **64** into the on-chip memory of the processing unit **62** as well as the pre-calculation of a period of an appropriate sinusoid to be used for current injection. Before the calibration

table is used for impedance calibration, the calibration table is screened for the integrity of the calibration values. Any problem with the calibration table results in an error code being returned to the DAS module in place of the calibrated impedance data. The processing unit **62** can also send the calibration data to the processing device **12**.

[00160] The DAF module generates the input current signal by writing a digital control signal to the DAC **70** which in turn provides a corresponding analog signal to the current generator **58**. The digital control signal comprises a pre-calculated sinusoidal period that is repeated, sample-by-sample, for a predetermined number of periods. In one embodiment, the current generator **58** converts 16 samples/cycle at frequencies below 75 kHz and 8 samples/cycle at frequencies above 75 kHz. The impedance module **20** then sends the generated current signal to the selected electrodes.

[00161] The DAF module directs data acquisition by instructing the ADC **68** to sample a data value between each converted output of the DAC **70** to the current generator **76**. The ADC **68** alternates between acquiring a differential voltage data sample and a current data sample. Accordingly, in this embodiment, the data acquisition sampling rate is half the stimulus (i.e. current injection) sampling rate. For higher frequencies, and in other cases where higher acquisition sampling rates are required for data acquisition, all current samples can be acquired first, followed by all voltage samples. In the second case, the data acquisition occurs for twice the number of sinusoidal periods. The total number of acquired data samples in both cases is exactly the same.

[00162] The DAF module calculates an impedance value at a particular frequency by either performing a decimation-in-time FFT to acquire the complex impedance at each frequency or performing a simple correlation with a pre-defined sinusoid with the stimulus sinusoid phase shifted by 45° to calculate the real and imaginary components of the voltage for a certain frequency component. The resulting complex voltage value is divided by the complex current value to produce the raw impedance results. In addition,

Bartlett, Hamming, Hanning, and Blackman windows can be applied to the signals before further processing. When the FFT is used, spectral information of the voltage and current waveform can be obtained to calculate the total harmonic distortion of the voltage measurement, and, by using the second and third harmonics, to determine whether saturation of the measured voltage signals has occurred. The spectral information can also be used to determine the magnitude and phase of each spectral component of the voltage and current signals, from which can be calculated the complex impedance at a frequency of interest (Fo) using the relationships: $|Z_{Fo}| = |V_{Fo}|/|I_{Fo}|$ and $\arg(Z_{Fo}) = \arg(V_{Fo}) - \arg(I_{Fo})$ where | | denotes magnitude and arg( ) denotes phase.

[00163] The magnitude of the raw impedance, as calculated above, directly reflects the magnitude of the measured voltage signal as acquired by the ADC **68**. Accordingly, if the measured voltage signal is too large, then the ADC **68** will saturate. Alternatively, if the measured voltage signal is too small, then the ADC **68** will use fewer bits in its conversion and the resulting measurements will be less accurate. In order to maximize the number of bits used in data conversion while preventing saturation, an automatic gain control algorithm is used in conjunction with the programmable gain unit **74**. When a raw impedance value is too large, the gain of the programmable gain unit **74** is reduced, and the load is re-measured. When a raw impedance value is too small, the gain of the programmable gain unit **74** is increased and the load is re-measured. Saturation can be determined by analysis of the second and third harmonics of the measured voltage signals (the second harmonic identifies slew-rate limiting and the third identifying clipping).

[00164] It should be understood that the computing device **12**, the main module **18** and the front end-module **22** described herein illustrate a particular application of the impedance module **20**. Other embodiments are possible in which the components of the computing device **12**, main module **18** and front-end module **22** are different. Accordingly, it should be understood that the impedance module **20** is a stand-alone device which can be used to measure impedance values. The impedance module **20** simply requires connection

leads to provide the stimulus current to a load and connection loads to receive the resulting voltages.

[00165] It should also be understood that various modifications can be made to the embodiments described and illustrated herein, without departing from the present invention, the scope of which is defined in the appended claims. For example, although emphasis has been placed on describing a system for diagnosing breast cancer, the principles of the present invention can also be advantageously applied to other diseases of other body parts. In addition, the main module **18**, the impedance module **20** and the front-end module **22** may be integrated with the computing device **12** to form a single unit.